What is claimed is:

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1. A capacitor, comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer intermediate the dielectric layer and one of the first and second electrodes.

2. The capacitor according to claim 1, wherein the one electrode is a tungsten nitride and the buffer layer is a tungsten oxide.

3. The capacitor according to claim 2, wherein the dielectric layer is a tantalum oxide.

4. The capacitor according to claim 1, wherein the buffer layer has a orthorhomic crystalline structure.

5. A capacitor, comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

a tungsten trioxide buffer layer interposed between the dielectric layer and one of the first and second electrodes.

6. The capacitor according to claim 5, wherein the buffer layer has a orthorhomic crystalline structure.

7. The capacitor according to claim 5, wherein the one electrode includes tungsten.

8. The capacitor according to claim 7, wherein the buffer layer is grown by oxidizing the one electrode.

9. A capacitor, comprising:
a first electrode;
a second electrode;
a dielectric layer interposed between the first electrode and the second electrode; and
a metal oxide buffer layer interposed between the dielectric layer and one of the first and second electrodes, wherein the metal oxide buffer layer includes a refractory metal.

10. The capacitor according to claim 9, wherein the buffer layer is of the formula MO_x, and M is a metal component from a group consisting of tungsten, tantalum, zirconium, and hafnium.

11. The capacitor according to claim 9, wherein the buffer layer has a orthorhomic crystalline structure.

12. A vertical capacitor, comprising:
a bottom electrode;
a top electrode positioned above the bottom electrode;
a dielectric layer interposed between the top electrode and the bottom electrode; and
a metal oxide buffer layer intermediate the dielectric layer and the bottom electrode.

13. The capacitor according to claim 12, wherein the bottom electrode is a tungsten nitride and the buffer layer is a tungsten oxide.

14. The capacitor according to claim 13, wherein the dielectric layer is a tantalum oxide.

15. The capacitor according to claim 12, wherein the buffer layer has a orthorhomic crystalline structure.

16. A capacitor, comprising:

a bottom electrode;

a top electrode;

a dielectric layer interposed between the top electrode and the bottom electrode; and

a metal oxide buffer layer intermediate the dielectric layer and the bottom electrode, wherein the metal in the buffer layer is a refractory metal.

17. The capacitor according to claim 16, wherein the metal in the buffer layer is tungsten.

18. The capacitor according to claim 17, wherein the bottom electrode comprises a metal nitride, and the metal in the bottom electrode is a refractory metal.

19. The capacitor according to claim 18, wherein the bottom electrode comprises tungsten nitride.

20 A capacitor, comprising:

a bottom electrode;

a top electrode;

a dielectric layer interposed between the top electrode and the bottom electrode; and

a metal oxide buffer layer intermediate the dielectric layer and the bottom electrode, wherein the bottom electrode comprises a metal nitride having a metal component which is the same as the metal component of the metal oxide buffer layer.

21. The capacitor according to claim 20, wherein the dielectric layer comprises tantalum oxide.

22. The capacitor according to claim 21, wherein the metal component of the bottom electrode and the buffer layer includes tungsten.

23. A capacitor, comprising:

a bottom electrode;

a top electrode;

a dielectric layer interposed between the bottom electrode and the top electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the bottom electrode and the top electrode;

wherein at least one electrode selected from the group consisting of the bottom electrode and the top electrode comprises tungsten nitride.

24. The capacitor according to claim 23, wherein the dielectric layer is a metal oxide of a different type than the buffer layer.

25. A capacitor, comprising:

a first electrode;

a second electrode;

a tantalum oxide dielectric layer interposed between the bottom electrode and the top electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the bottom electrode and the top electrode;

wherein at least one electrode is selected from the group consisting of the bottom electrode and the top electrode includes tungsten nitride.

26. A capacitor, comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer intermediate the dielectric layer and one of the first and second electrodes, wherein the metal oxide buffer layer has an orthorhomic crystal structure.

27. The capacitor according to claim 26, wherein the metal in the buffer layer is tungsten.

28. A capacitor, comprising:

a bottom electrode;

a top electrode;

a dielectric layer interposed between the top electrode and the bottom electrode; and

an annealed metal oxide buffer layer intermediate the dielectric layer and the bottom electrode.

29. The capacitor according to claim 28, wherein the bottom electrode comprises a metal nitride and has a metal component which is the same as the metal component of the metal oxide buffer layer.

30. A capacitor, comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer intermediate the dielectric layer and one of the first and second electrodes;

wherein the buffer layer has a dielectric constant greater than the dielectric layer.

31. The capacitor according to claim 30, wherein the one of the first and second electrodes has a metal component which is the same as the metal component of the buffer layer.

32. The capacitor according to claim 30, wherein the buffer layer has an orthorhomic crystalline structure.

33. A method of forming a capacitor, comprising:

forming a bottom electrode layer;

forming a metal oxide buffer layer overlying the bottom electrode layer;

forming a dielectric layer overlying the metal oxide buffer layer; and

forming a top electrode layer overlying the dielectric layer.

34. The method of claim 33, further comprising patterning the top electrode layer, the buffer layer, the dielectric layer, and the bottom electrode layer to define the capacitor.

35. The method of claim 33, wherein the method is performed in the order presented.

36. A method of forming a capacitor, comprising:

forming a bottom electrode layer;

forming a metal oxide buffer layer overlying the bottom electrode layer;

annealing the buffer layer;

forming a dielectric layer overlying the metal oxide buffer layer; and

forming a top electrode layer overlying the dielectric layer.

37. The method of claim 36, further comprising patterning the top electrode layer, the buffer layer, the dielectric layer, and the bottom electrode layer to define the capacitor.

38. The method of claim 36, wherein the method is performed in the order presented.

39. A method of forming a capacitor, comprising:

forming a bottom electrode layer on a substrate;

oxidizing the bottom electrode layer to form a metal oxide buffer layer overlying the bottom electrode layer;

forming a dielectric layer overlying the metal oxide buffer layer; and

forming a top electrode layer overlying the dielectric layer.

40. The method of claim 39, wherein the method is performed in the order presented.

41. A method of forming a capacitor, comprising:
forming a bottom electrode layer on a substrate;
oxidizing the bottom electrode layer to form a metal oxide buffer layer overlying the bottom electrode layer;
annealing the buffer layer;
forming a dielectric layer overlying the metal oxide buffer layer; and
forming a top electrode layer overlying the dielectric layer.

42. The method of claim 41, wherein the method is performed in the order presented.

43. The method of claim 42, wherein the bottom electrode is deposited by chemical vapor deposition, and the top electrode is deposited by chemical vapor deposition.

44. The method of claim 41, wherein the dielectric layer is formed to a thickness of about 80 Å.

45. A method of forming a capacitor, comprising:
forming a bottom electrode layer on a substrate;
oxidizing the bottom electrode layer to form a metal oxide buffer layer overlying the bottom electrode layer;
annealing the buffer layer at about 700 degrees Celsius;
forming a dielectric layer overlying the metal oxide buffer layer; and
forming a top electrode layer overlying the dielectric layer.

46. The method of claim 45, wherein the buffer layer is annealed for about one minute.

47. The method of claim 45, wherein the buffer layer is annealed in an N_2 ambient.

48. A method of forming a capacitor, comprising:
forming a first electrode layer;

forming a second electrode layer;

forming a dielectric layer interposed between the first electrode layer and the second electrode layer; and

forming a metal oxide buffer layer intermediate the dielectric layer and one of the first and second electrode layers.

49. The method of claim 48, wherein forming the buffer layer includes oxidizing the one of the first and second electrode layers to form the buffer layer and thereafter high temperature annealing the buffer layer.

50. A method of forming a capacitor, comprising:

forming an insulating layer on a substrate;

forming an opening in the insulating layer, wherein the opening has a bottom portion overlying an exposed portion of the substrate and sidewall portions defined by the insulating layer;

forming a bottom electrode layer overlying the insulating layer, the exposed portion of the substrate and the sidewall portions;

forming a metal oxide buffer layer overlying the bottom electrode layer;

forming a dielectric layer overlying the metal oxide buffer layer;

forming a top electrode layer overlying the dielectric layer; and

patterning the top electrode layer, dielectric layer, metal oxide buffer layer and bottom electrode layer to thereby define the capacitor.

51. The method of claim 50, wherein forming the bottom electrode layer comprises forming a layer of metal nitride.

52. The method of claim 51, wherein forming the bottom electrode layer comprises forming a layer of tungsten nitride.

53. The method of claim 52, wherein forming the metal oxide buffer layer comprises oxidizing the bottom electrode layer to form the metal oxide buffer layer, and annealing the metal oxide buffer layer.

54. The method of claim 50, wherein the metal oxide buffer layer is annealed at a temperature of over 650 degrees Celsius.

55. The method of claim 50, wherein the metal oxide buffer layer is annealed at a temperature of at least 700 degrees Celsius.

56. A method of forming a capacitor, comprising:

forming an insulating layer on a substrate;

forming an opening in the insulating layer, wherein the opening has a bottom portion overlying an exposed portion of the substrate and sidewall portions defined by the insulating layer;

forming a tungsten nitride bottom electrode layer overlying the insulating layer, the exposed portion of the substrate and the sidewall portions;

forming a tungsten oxide buffer layer overlying the bottom electrode layer;

forming a dielectric layer overlying the metal oxide buffer layer;

forming a top electrode layer overlying the dielectric layer; and

patterning the top electrode layer, dielectric layer, buffer layer and bottom electrode layer to thereby define the capacitor.

57. A method of forming a capacitor, comprising:

forming an insulating layer on a substrate;

forming an opening in the insulating layer, wherein the opening has a bottom portion overlying an exposed portion of the substrate and sidewall portions defined by the insulating layer;

forming a tungsten nitride bottom electrode layer overlying the insulating layer, the exposed portion of the substrate and the sidewall portions;

oxidizing the bottom electrode layer to form a tungsten oxide buffer layer overlying the bottom electrode layer;

annealing the buffer layer to an orthorhomic crystal lattice;

forming a dielectric layer overlying the buffer layer;

forming a top electrode layer overlying the dielectric layer; and

patterning the top electrode layer, dielectric layer, buffer layer and bottom electrode layer to thereby define the capacitor.

58. The method according to claim 57, wherein annealing the buffer layer includes annealing at a temperature of at least 700 degrees Celsius.

59. A method of forming a capacitor, comprising:

forming an insulating layer on a substrate;

forming an opening in the insulating layer, wherein the opening has a bottom portion overlying an exposed portion of the substrate and sidewall portions defined by the insulating layer;

depositing a tungsten nitride bottom electrode layer overlying the insulating layer, the exposed portion of the substrate and the sidewall portions;

oxidizing the bottom electrode layer to form a tungsten oxide buffer layer overlying the bottom electrode layer;

annealing the buffer layer at a temperature of at least 700 degrees Celsius to have an orthorhomic crystal lattice;

depositing a tantalum oxide dielectric layer overlying the buffer layer;

depositing a metal top electrode layer overlying the dielectric layer; and

patterning the top electrode layer, dielectric layer, buffer layer and bottom electrode layer to thereby define the capacitor.

60. The method of claim 59, wherein the metal top electrode includes a noble metal.

61. The method of claim 60, wherein the top electrode includes a platinum alloy.

62. A method of forming a capacitor, comprising:

forming a bottom electrode layer;

forming a orthorhomic crystal structured buffer layer overlying the bottom electrode layer;

forming a dielectric layer overlying the buffer layer; and

forming a top electrode layer overlying the dielectric layer.

63. The method of claim 62, further comprising patterning the top electrode layer, the buffer layer, the dielectric layer, and the bottom electrode layer to define the capacitor.

64. The method of claim 62, wherein the method is performed in the order presented.

65. A method of forming a capacitor, comprising:

forming a first electrode layer, wherein the first electrode layer comprises a metal nitride having a metal component;

forming a buffer layer overlying the first electrode layer, wherein the buffer layer comprises a metal oxide having a composition of the form MO_x, wherein M is a metal component selected from the group consisting of chromium, cobalt, hafnium, iridium, molybdenum, niobium, osmium, rhenium, rhodium, ruthenium, tantalum, titanium, tungsten, vanadium and zirconium;

forming a dielectric layer overlying the buffer layer;

forming a second electrode layer overlying the buffer layer, wherein the second electrode layer comprises a metal nitride having a metal component; and

patterning the second electrode layer, dielectric layer, buffer layer and first electrode layer to thereby define the capacitor.

66. The method of claim 65, wherein the metal component of the first electrode layer is tungsten.

67. The method of claim 67, wherein the metal component M of the buffer layer is selected to be the same as the metal component of the first electrode layer.

68. The method of claim 66, wherein the dielectric layer comprises a metal oxide dielectric material.

69. The method of claim 66, wherein the method is performed in the order presented.

70. A method of forming a capacitor, comprising:
forming a bottom electrode layer;
forming a metal oxide buffer layer overlying the bottom electrode layer;
forming a dielectric layer having a dielectric constant less than the buffer overlying the buffer layer; and
forming a top electrode layer overlying the dielectric layer.

71. The method of claim 70, further comprising patterning the top electrode layer, the buffer layer, the dielectric layer, and the bottom electrode layer to define the capacitor.

72. The method of claim 70, wherein the method is performed in the order presented.

73. A semiconductor die, comprising:
an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:
a first electrode;
a second electrode;
a dielectric layer interposed between the first electrode and the second electrode; and
at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first

electrode and the second electrode.

74. A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode.

75. A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a metal oxide dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

wherein at least one electrode selected from the group consisting of the first electrode and the second electrode comprises tungsten nitride.

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76. A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a tungsten nitride second electrode;

a metal oxide dielectric layer interposed between the first electrode and the second electrode; and

a tungsten oxide buffer layer is interposed between the dielectric layer and the second electrode.

77. A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a tungsten nitride second electrode;

a metal oxide dielectric layer interposed between the first electrode and the second electrode; and

a high temperature annealed, tungsten oxide buffer layer is interposed between the dielectric layer and the second electrode.

78. The semiconductor die according to claim 77, wherein the high temperature annealed buffer layer is annealed at least 700 degrees Celsius and has an orthorhomic crystal structure.

79. A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

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a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer is interposed between the dielectric layer and the second electrode,

wherein the buffer layer has an orthorhomic crystal lattice structure.

80. A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer is interposed between the dielectric layer and the second electrode,

wherein the buffer layer has a dielectric constant greater than the dielectric layer.

81. A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

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a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

82. The memory device according to claim 81, wherein the electrode selected from the group consisting of the first electrode and the second electrode has a metal component that is the same as the metal component of the buffer layer.

83. A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

84. A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a metal oxide dielectric layer interposed between the first electrode and the second electrode; and

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at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, wherein at least one electrode selected from the group consisting of the bottom electrode of the capacitor and the top electrode of the capacitor comprises tungsten nitride;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

85. A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having an orthorhomic crystalline structure;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

86. A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

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a dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having a dielectric constant greater than the dielectric layer;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

87. A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

at least one, high temperature annealed, metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

88. A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

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a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

89. The module according to claim 88, wherein the electrode selected from the group consisting of the first electrode and the second electrode includes a metal component that is the same as the metal component of the buffer layer.

90. A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

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at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the bottom electrode and the top electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

91. A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

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a metal oxide dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having a dielectric constant greater than the dielectric layer;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit

wherein at least one electrode selected from the group consisting of the bottom electrode of the capacitor and the top electrode of the capacitor comprises tungsten nitride.

92. A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and

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an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having an orthorhomic crystalline structure;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

93. A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

at least one, high temperature annealed metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

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an address decoder circuit coupled to the row access circuit and the column access circuit.

94. A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

95. The system according to claim 94, wherein the electrode selected from the group consisting of the first electrode and the second electrode includes a metal component that is the same as the metal component of the buffer layer.

96. A memory system, comprising:

a controller;

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a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

97. A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having an orthorhomic crystalline structure;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

98. A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having a dielectric constant greater than the dielectric layer;

a row access circuit coupled to the array of memory cells;

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a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

99. A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

at least one high temperature annealed, metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

100. An electronic system, comprising:

a processor; and

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a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode.

101. The system according to claim 100, wherein the electrode selected from the group consisting of the first electrode and the second electrode includes a metal component that is the same as the metal component of the buffer layer.

102. An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

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a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode.

103. An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the bottom electrode and the top electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

wherein the metal oxide buffer layer has an orthorhomic crystalline structure.

104. An electronic system, comprising:

a processor; and

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a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the bottom electrode and the top electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

wherein the metal oxide buffer layer has a dielectric constant greater than the dielectric constant of the dielectric layer.

105. An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

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a dielectric layer interposed between the bottom electrode and the top electrode; and

at least one high temperature annealed, metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode.

106. A capacitor, comprising:

an annealed bottom electrode;

a top electrode;

a dielectric layer interposed between the top electrode and the bottom electrode; and

an annealed metal oxide buffer layer intermediate the dielectric layer and the bottom electrode.

107. A method of forming a capacitor, comprising:

forming a bottom electrode layer;

annealing the bottom electrode layer;

forming a metal oxide buffer layer overlying the bottom electrode layer;

annealing the buffer layer;

forming a dielectric layer overlying the metal oxide buffer layer; and

forming a top electrode layer overlying the dielectric layer.

108. The method of claim 107, further comprising patterning the top electrode layer, the buffer layer, the dielectric layer, and the bottom electrode layer to define the capacitor.

109. The method of claim 108, wherein the method is performed in the order presented.

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110. A memory cell comprising a capacitor and an access device, wherein the capacitor includes:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer intermediate the dielectric layer and one of the first and second electrodes.

111. The memory cell according to claim 110, wherein the one electrode is a tungsten nitride and the buffer layer is a tungsten oxide.

112. The memory cell according to claim 110, wherein the buffer layer has a orthorhomic crystalline structure.

113. A memory cell comprising a capacitor and an access device, wherein the capacitor includes:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

a tungsten trioxide buffer layer interposed between the dielectric layer and one of the first and second electrodes.

114. The memory cell according to claim 113, wherein the one electrode includes tungsten.

115. The memory cell according to claim 114, wherein the buffer layer is grown by oxidizing the one electrode.

116. A memory cell comprising a capacitor and an access device, wherein the capacitor includes:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer interposed between the dielectric layer and one of the first and second electrodes, wherein the metal oxide buffer layer includes a refractory metal.

117. The memory cell according to claim 116, wherein the buffer layer is of the formula MO_x, and M is a metal component from a group consisting of tungsten, tantalum, zirconium, and hafnium.

118. A processor and a memory cell electrically connected to said processor, wherein said memory cell includes a capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer intermediate the dielectric layer and one of the first and second electrodes.

119. The memory cell according to claim 118, wherein the one electrode is a tungsten nitride and the buffer layer is a tungsten oxide.

120. The memory cell according to claim 118, wherein the buffer layer has a orthorhomic crystalline structure.

121. A processor and a memory cell electrically connected to said processor, wherein said memory cell includes a capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

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a tungsten trioxide buffer layer interposed between the dielectric layer and one of the first and second electrodes.

122. The memory cell according to claim 121, wherein the one electrode includes tungsten.

123. The memory cell according to claim 122, wherein the buffer layer is grown by oxidizing the one electrode.

124. A processor and a memory cell electrically connected to said processor, wherein said memory cell includes a capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer interposed between the dielectric layer and one of the first and second electrodes, wherein the metal oxide buffer layer includes a refractory metal.

125. The memory cell according to claim 124, wherein the buffer layer is of the formula MO_x, and M is a metal component from a group consisting of tungsten, tantalum, zirconium, and hafnium.

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